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uATX(243.84mm X 203.2mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Realtek RTM875N-632

HD Audio Codec:ALC887-VD-GR

LAN:RTL8111E 10/100/1000

IO: Fintek F71858AD

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:NCP5395 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *4

USB2.0 *10 (Rear*4 / Front*4)

USB3.0*2

On BOARD BUZZER



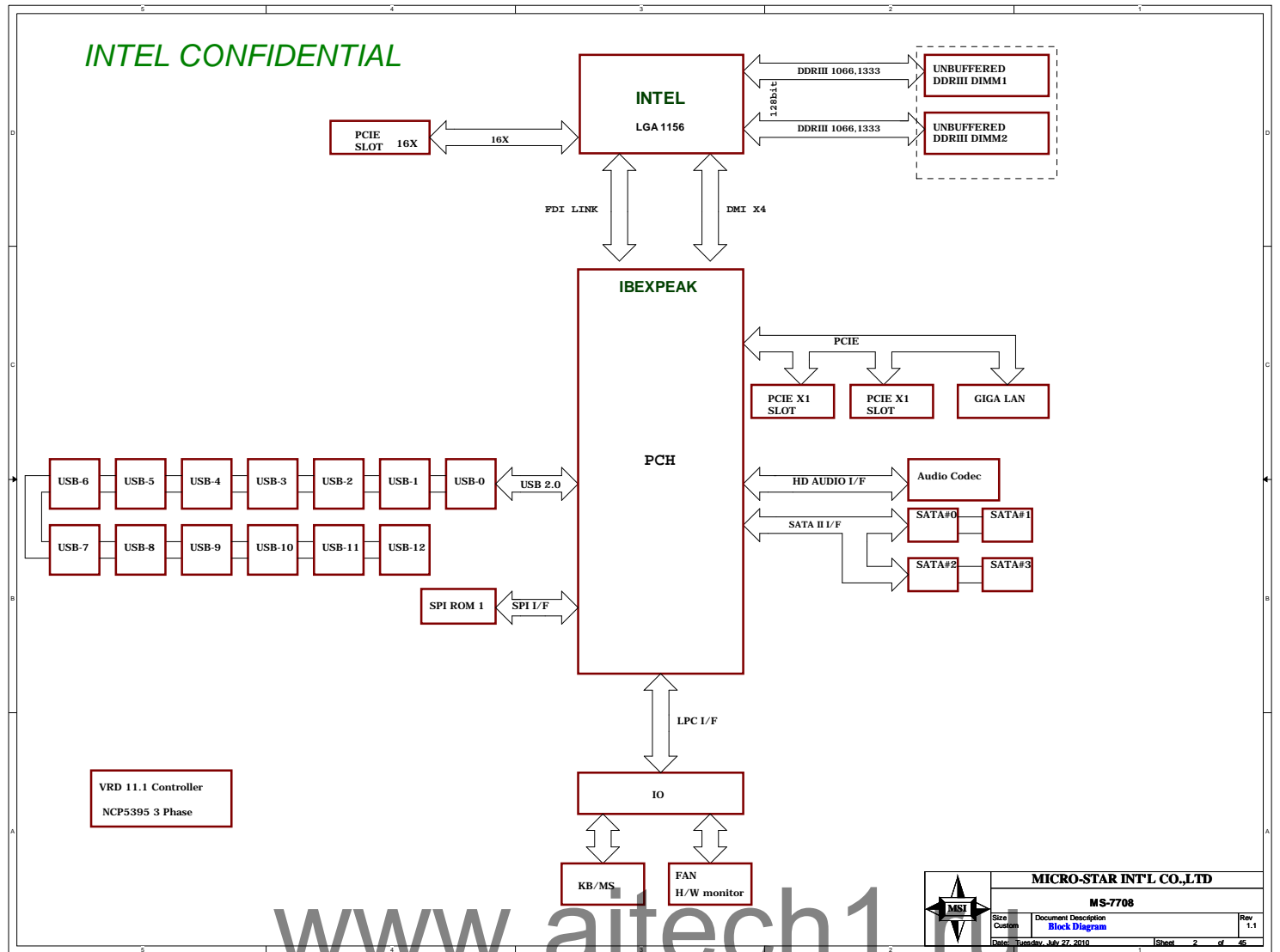
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DDR DIMM Config.

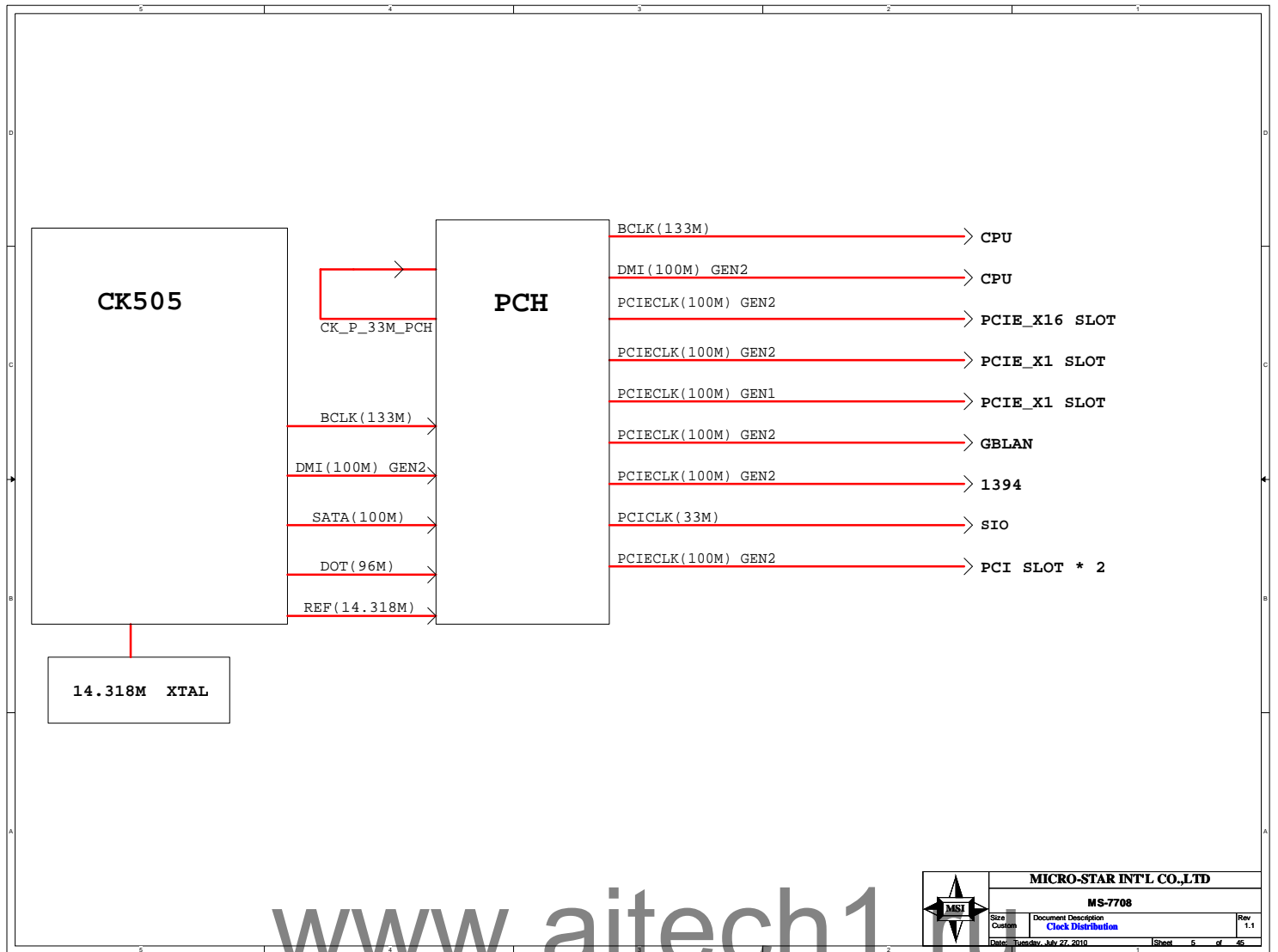
DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9:
USB PORT MAPPING SUBJECT TO CHANGES

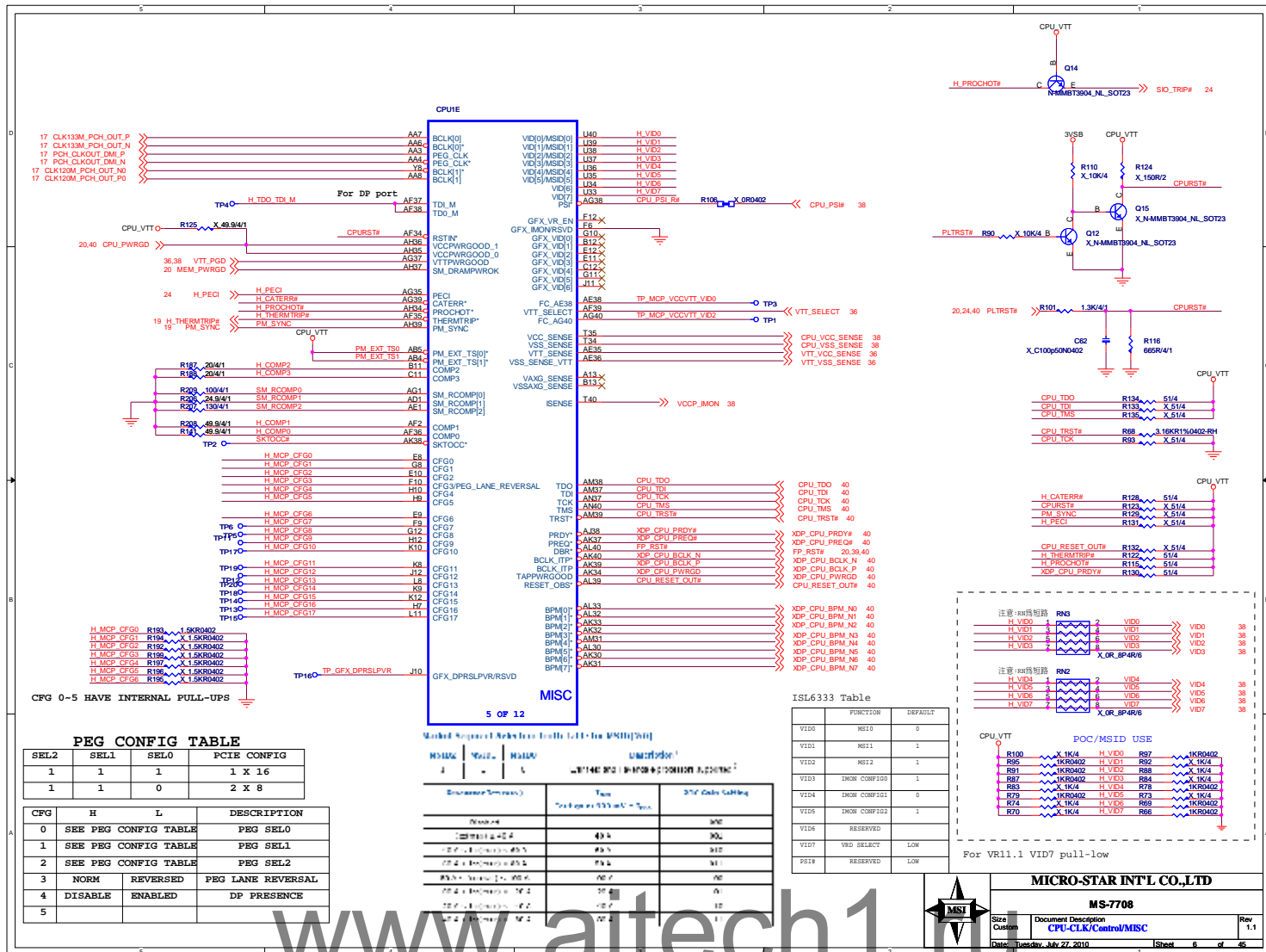
Controller	Port	Destination	max. USB Ports	Full Cap.	Over Current Protection
UHCI0, EHCI0	Port 0	Internal USB, Device F15.0	255	Y	Y
	Port 1	Internal USB, Device F15.0	255	Y	Y
UHCI1, EHCI1	Port 2	Internal USB, Device F15.0	255	Y	Y
	Port 3	Internal USB, Device F15.0	255	Y	Y
UHCI2, EHCI2	Port 4	Internal USB	255	Y	Y
	Port 5	Internal USB	255	Y	Y
UHCI3, EHCI3	Port 6	Internal USB	255	Y	Y
	Port 7	Internal USB	255	Y	Y
UHCI4, EHCI4	Port 8	Internal USB	255	Y	Y
	Port 9	Internal USB	255	Y	Y
UHCI5, EHCI5	Port 10	Internal USB	255	Y	Y
	Port 11	Internal USB	255	Y	Y
UHCI6, EHCI6	Port 12	Internal USB	255	Y	Y
	Port 13	Internal USB	255	Y	Y
UHCI7, EHCI7	Port 14	Internal USB	255	Y	Y
	Port 15	Internal USB	255	Y	Y

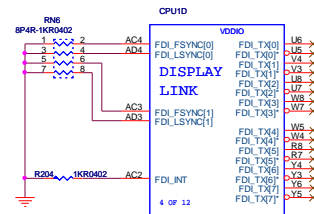
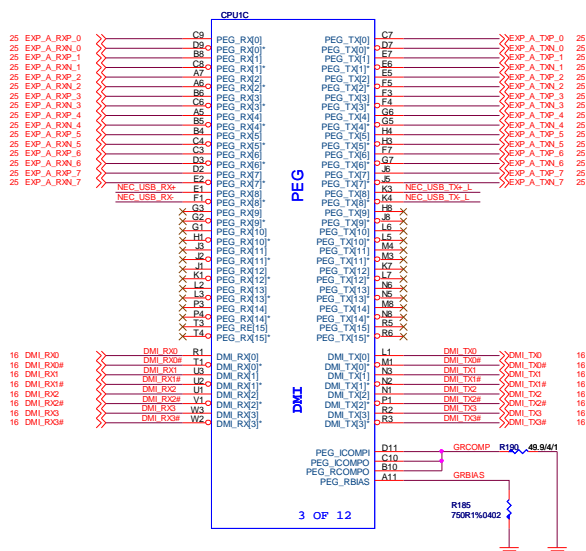
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24.24 Intel® Flexible Display Interface (Intel® FDI)

Table 24-36. Intel® Flexible Display Interface Signals

Signal	Type	Remarks	External Signal
FDI_LSYNC[0]	Input	Line Sync	FDI_LSYNC[0]
FDI_LSYNC[1]	Input	Line Sync	FDI_LSYNC[1]
FDI_TX[0:31]	Output	Display Data	FDI_TX[0:31]
FDI_RX[0:31]	Input	Display Data	FDI_RX[0:31]
FDI_TX[32:63]	Output	Display Data	FDI_TX[32:63]
FDI_RX[64:95]	Input	Display Data	FDI_RX[64:95]

Table 7-6. Haswell/ Lynnfield PCI Express® and DMI Compensation Routing Guidelines

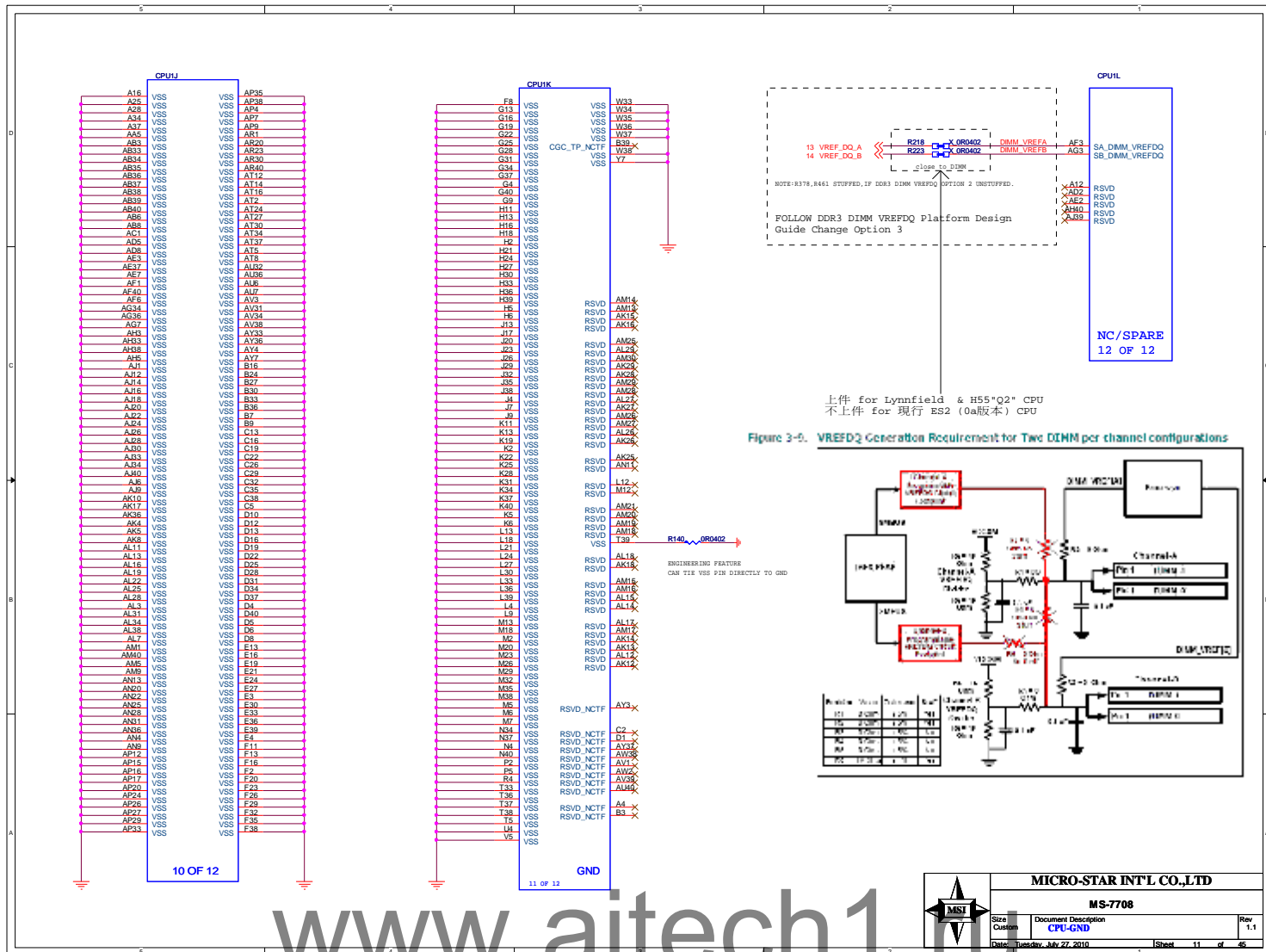
Signal Name	Width (W) / Spacing (S)	Length	Termination	Notes
PCI_EXP_B0	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B1	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B2	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B3	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B4	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B5	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B6	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B7	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B8	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B9	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B10	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B11	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B12	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B13	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B14	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B15	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B16	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B17	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B18	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B19	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B20	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B21	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B22	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B23	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B24	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B25	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B26	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B27	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B28	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B29	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B30	16 W / 16 S	10.0" ± 0.1"	100 Ω	
PCI_EXP_B31	16 W / 16 S	10.0" ± 0.1"	100 Ω	

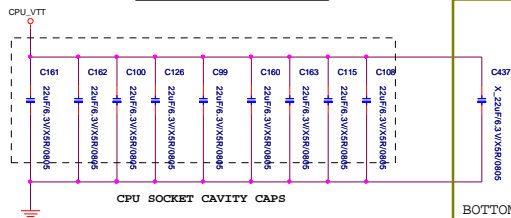
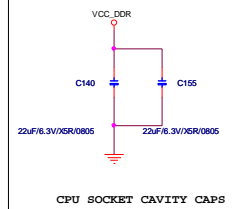
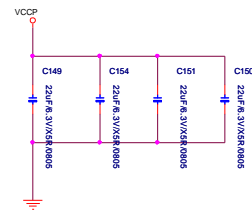
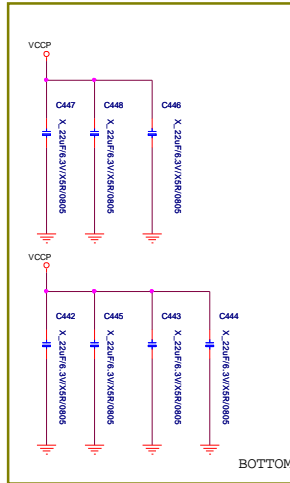
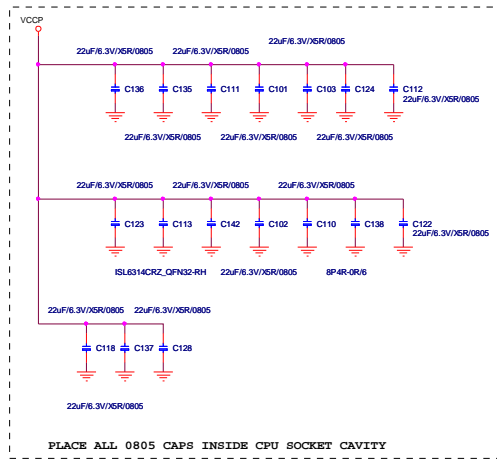


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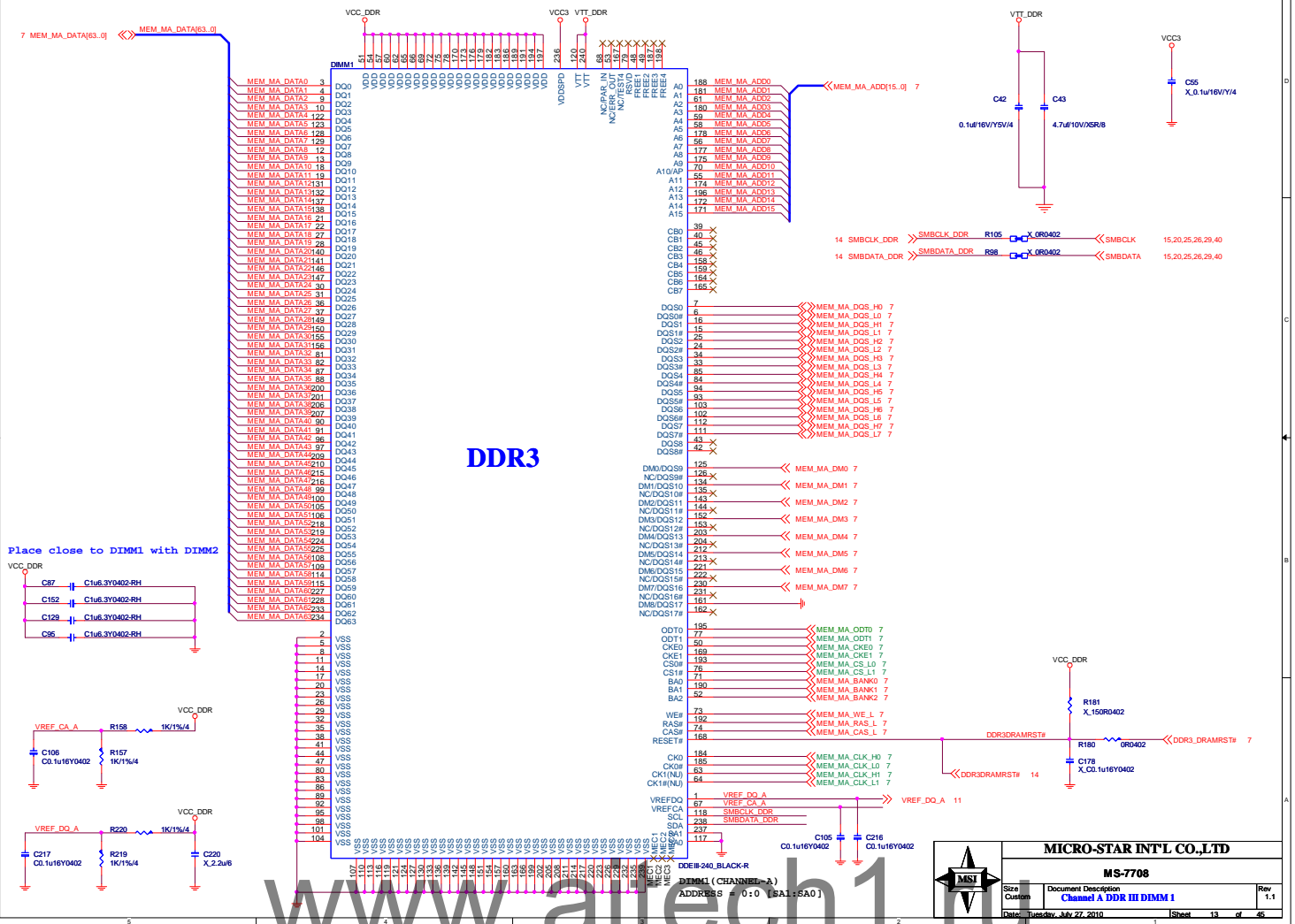
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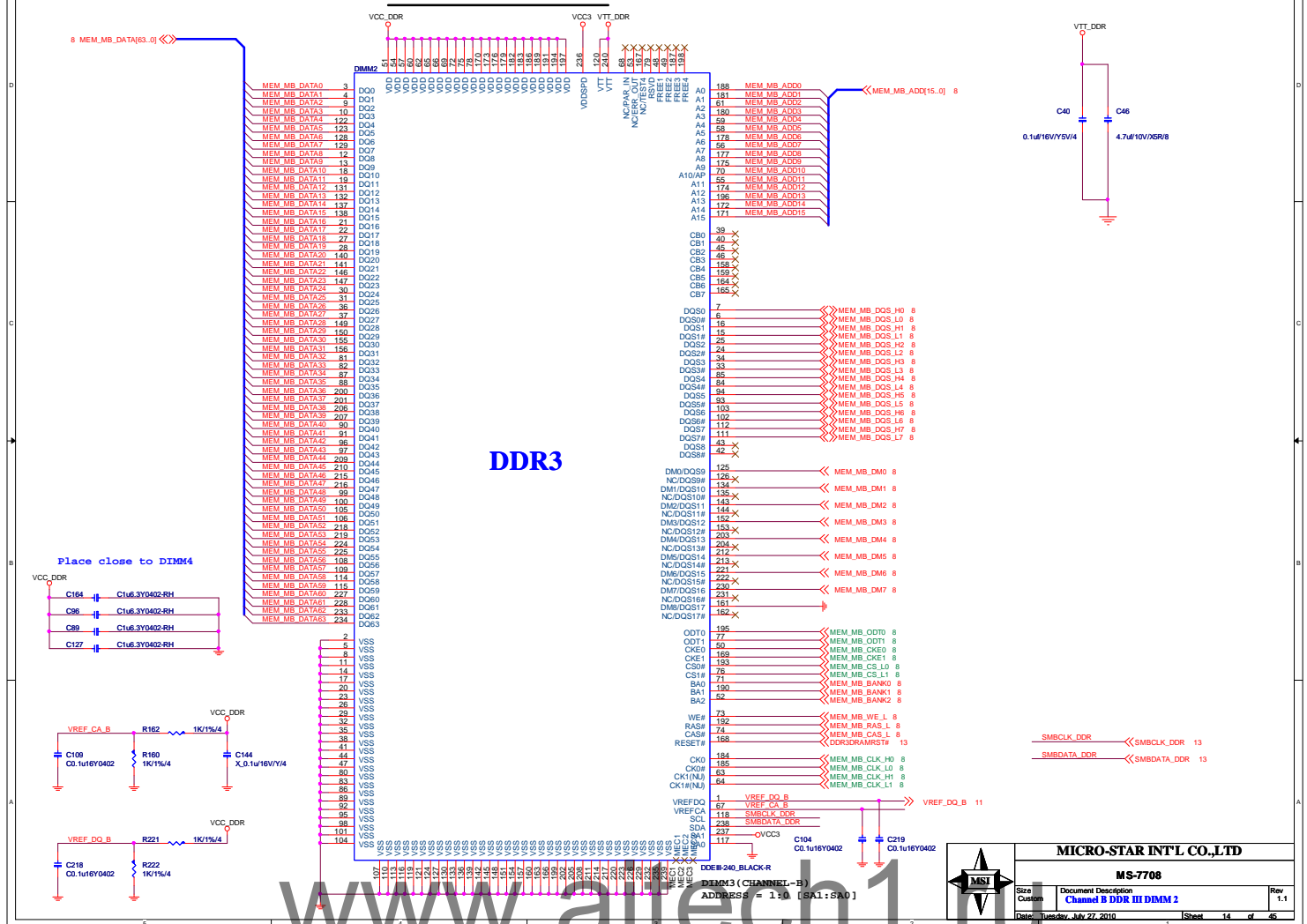


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DDRIII DIMM_A1

DDRIII DIMM_B1



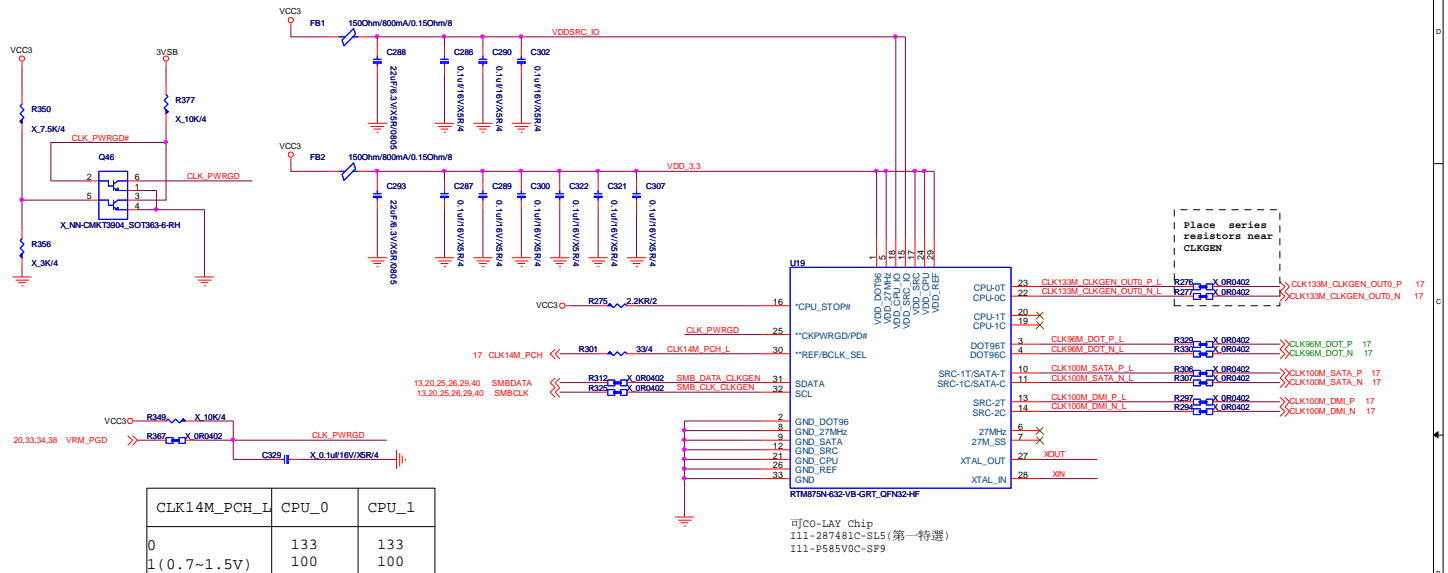
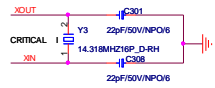
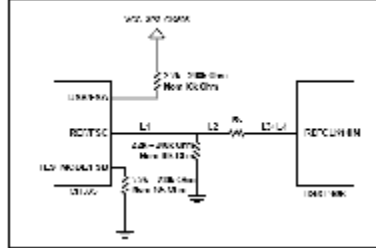
CLOCK Gen / RTM875N-632

Figure 9. LS, REFCLK Topology from C335 to Base Peak with DCCLK Frequency Strapping



CLOCK EMI CAPS: DEFAULT EMPTY

CLK14M_PCH_L	CPU_0	CPU_1
0	133	133
1(0.7~1.5V)	100	100

CLK14M_PCH_L C319 X_10pF/25V/7

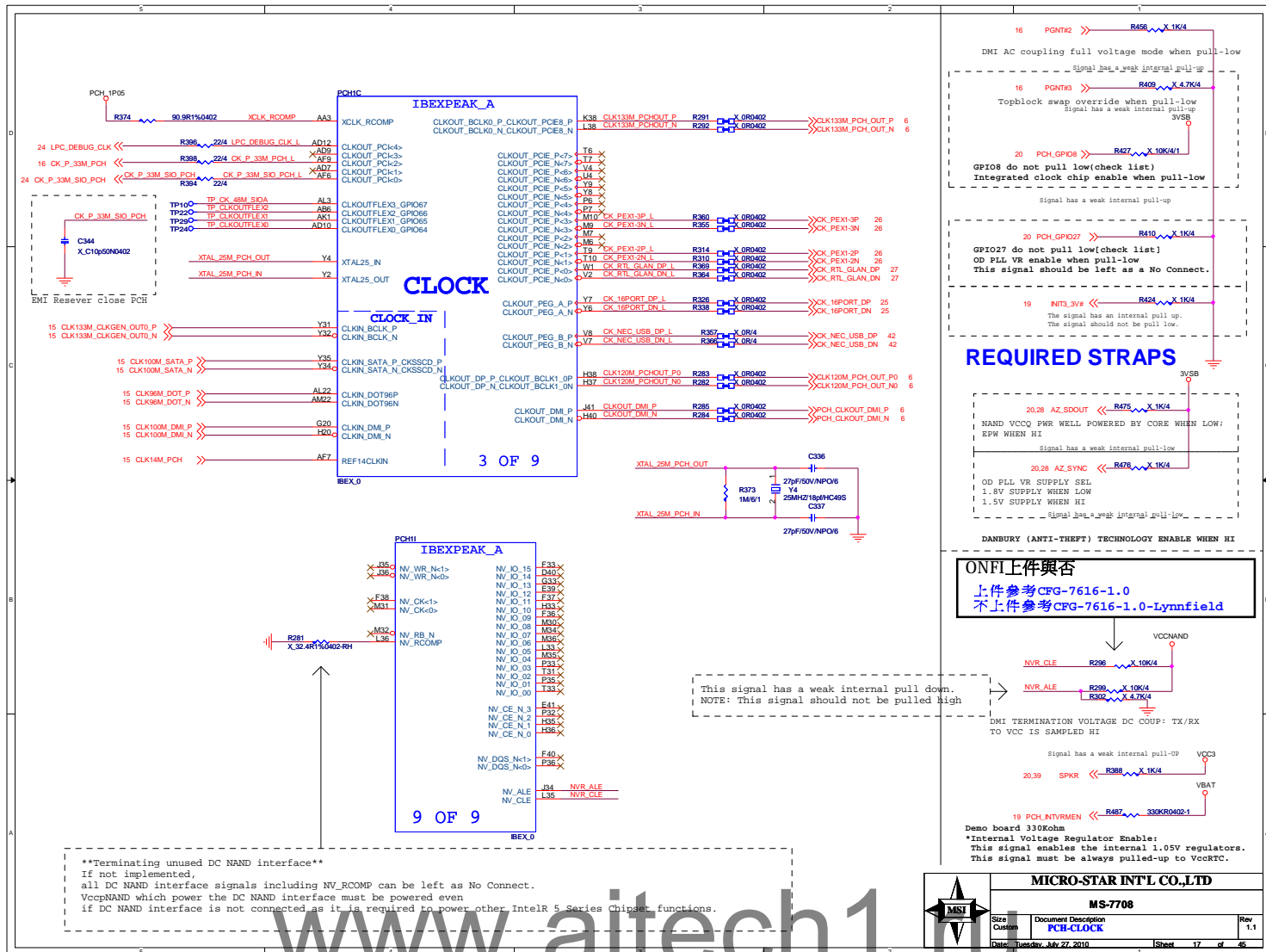


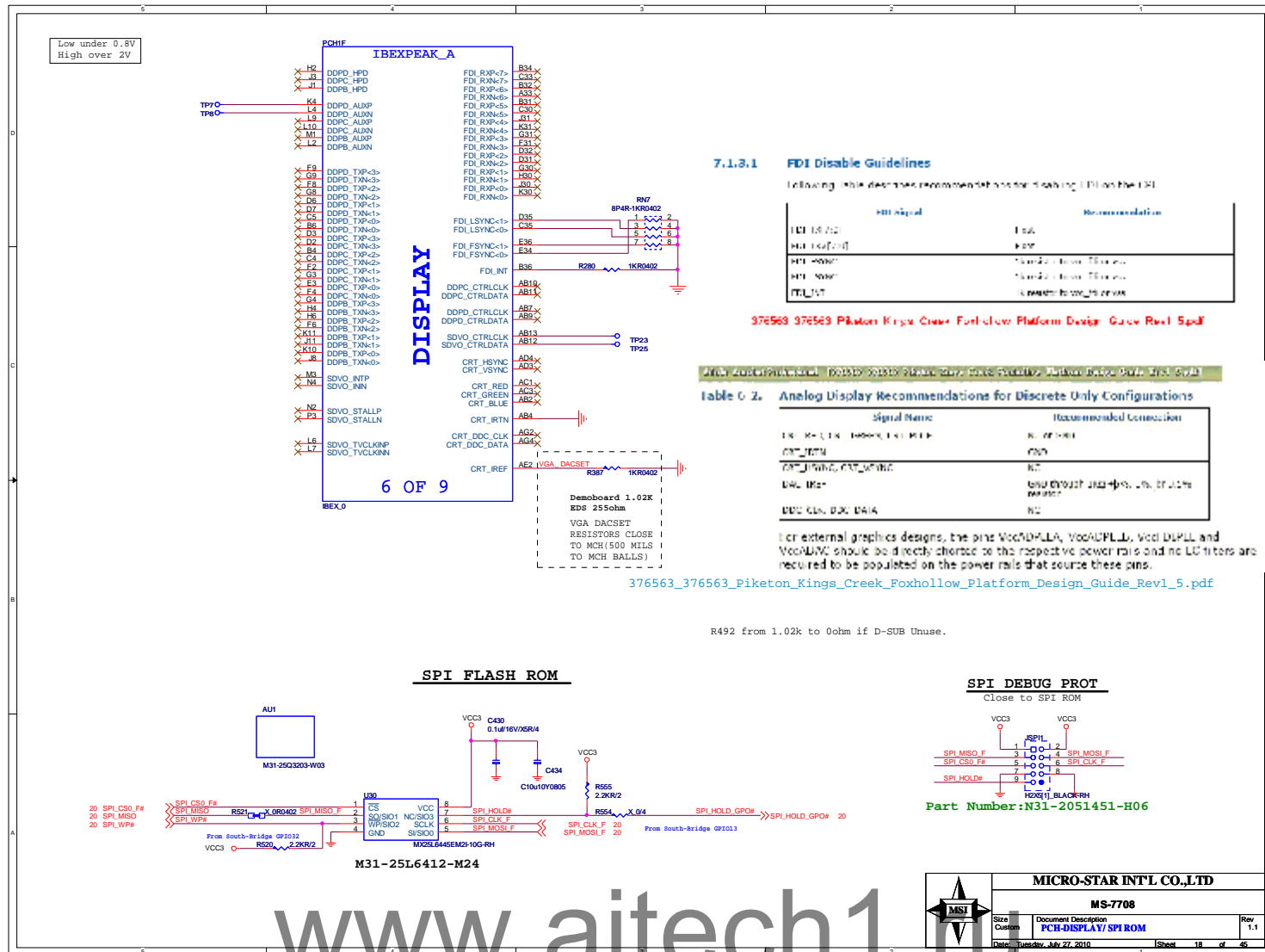
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7.1.3.1 FDI Disable Guidelines

Following table describes recommended connections for disabling FDI on the FSI.

FDI signal	Recommendation
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1.5.pdf

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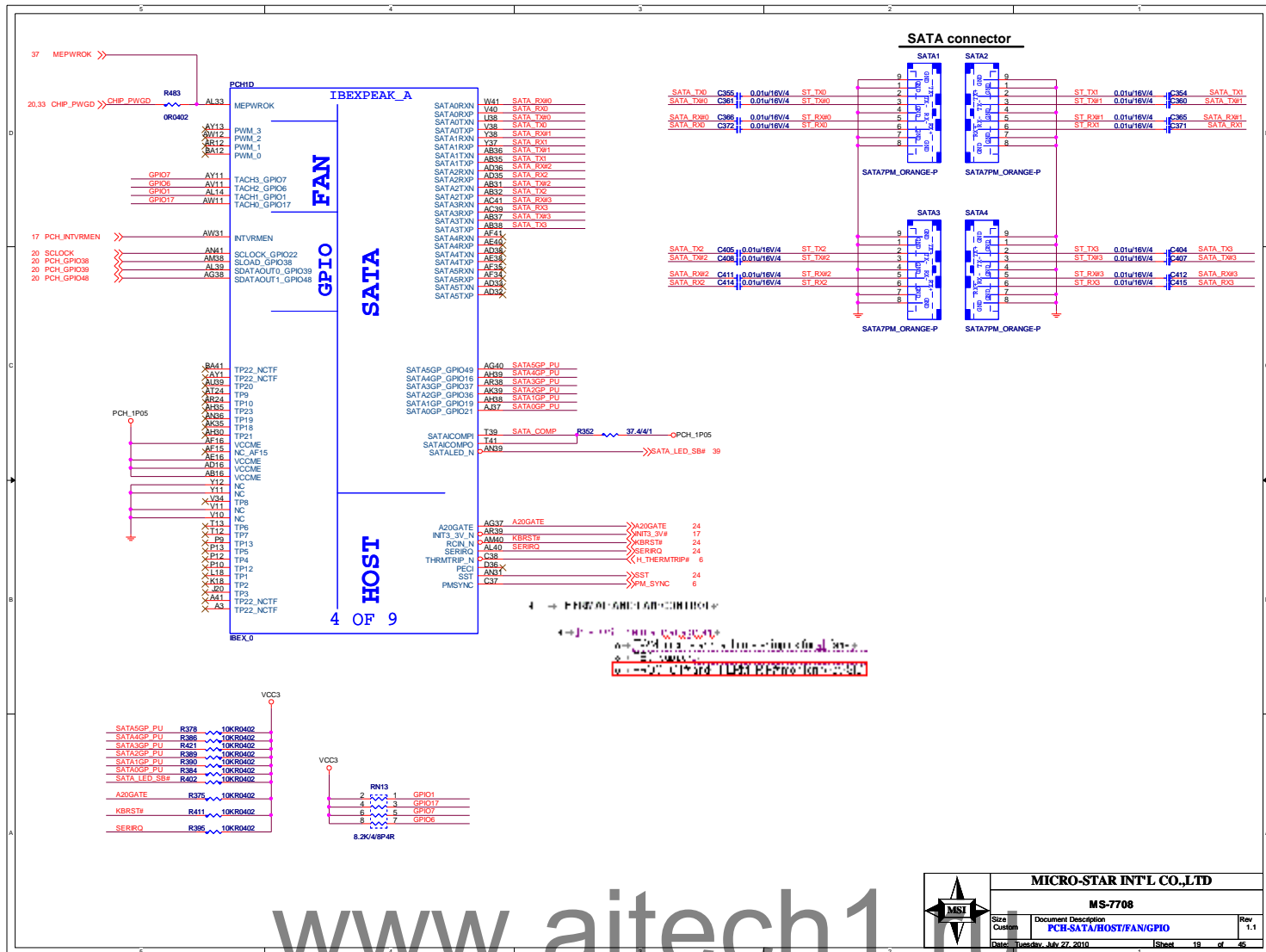
Table 6.2. Analog Display Recommendations for Discrete Only Configurations

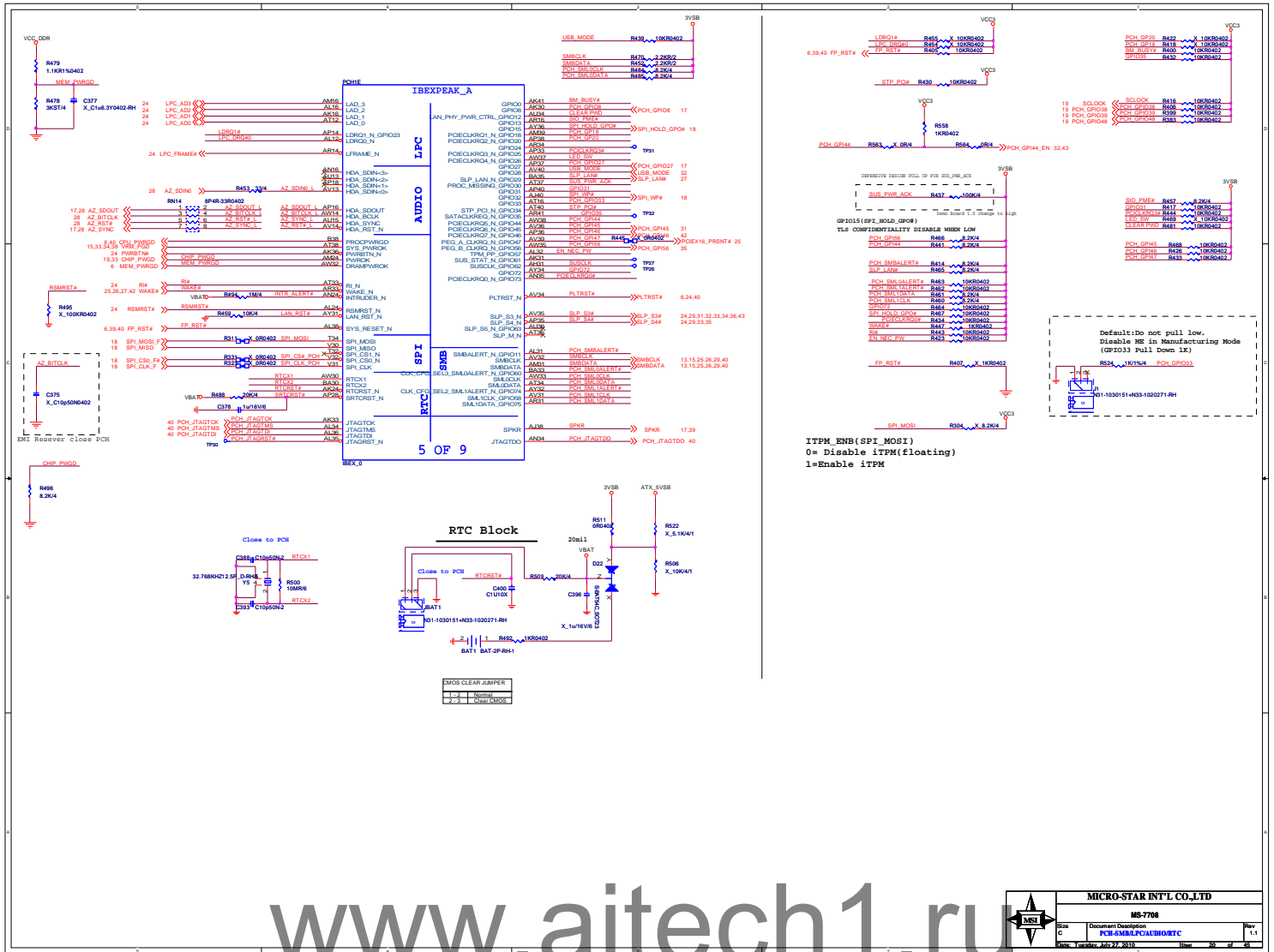
Signal Name	Recommended Connection
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k
FDI_16/12	1.5k

For external graphics designs, the pins VccADPALL, VccADPLL, VccADPLL and VccADPLL should be directly connected to the respective power rails and no LC filters are required to be populated on the power rails that source these pins.

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1.5.pdf

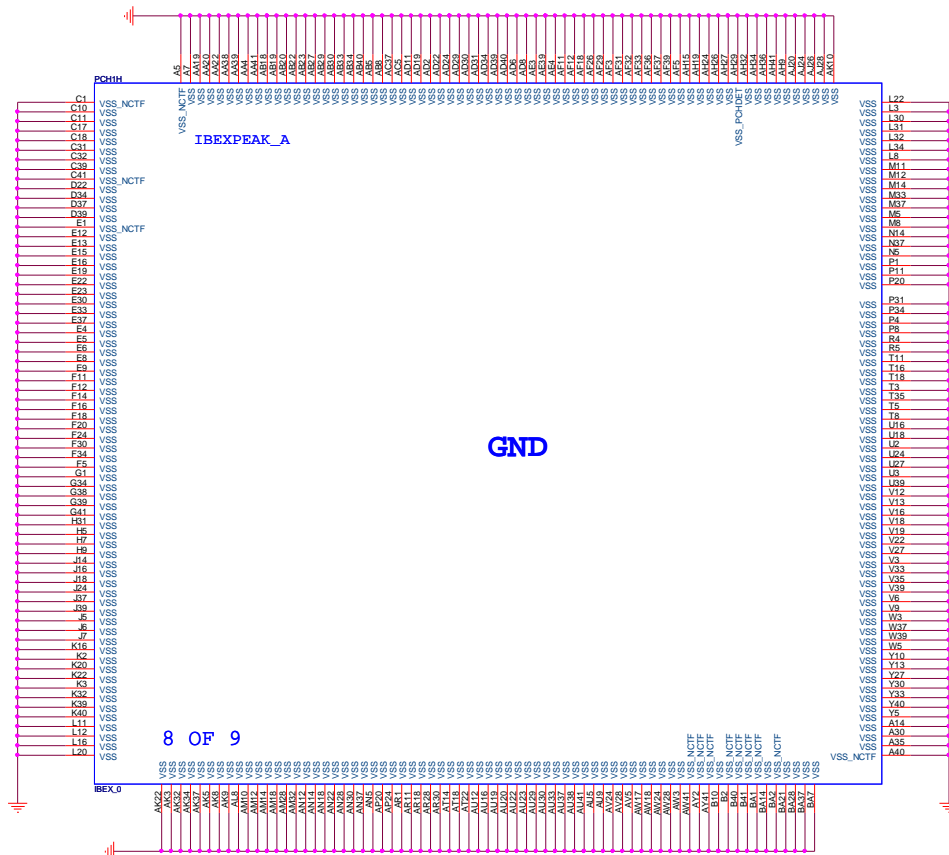
R492 from 1.02k to 0ohm if D-SUB Unuse.

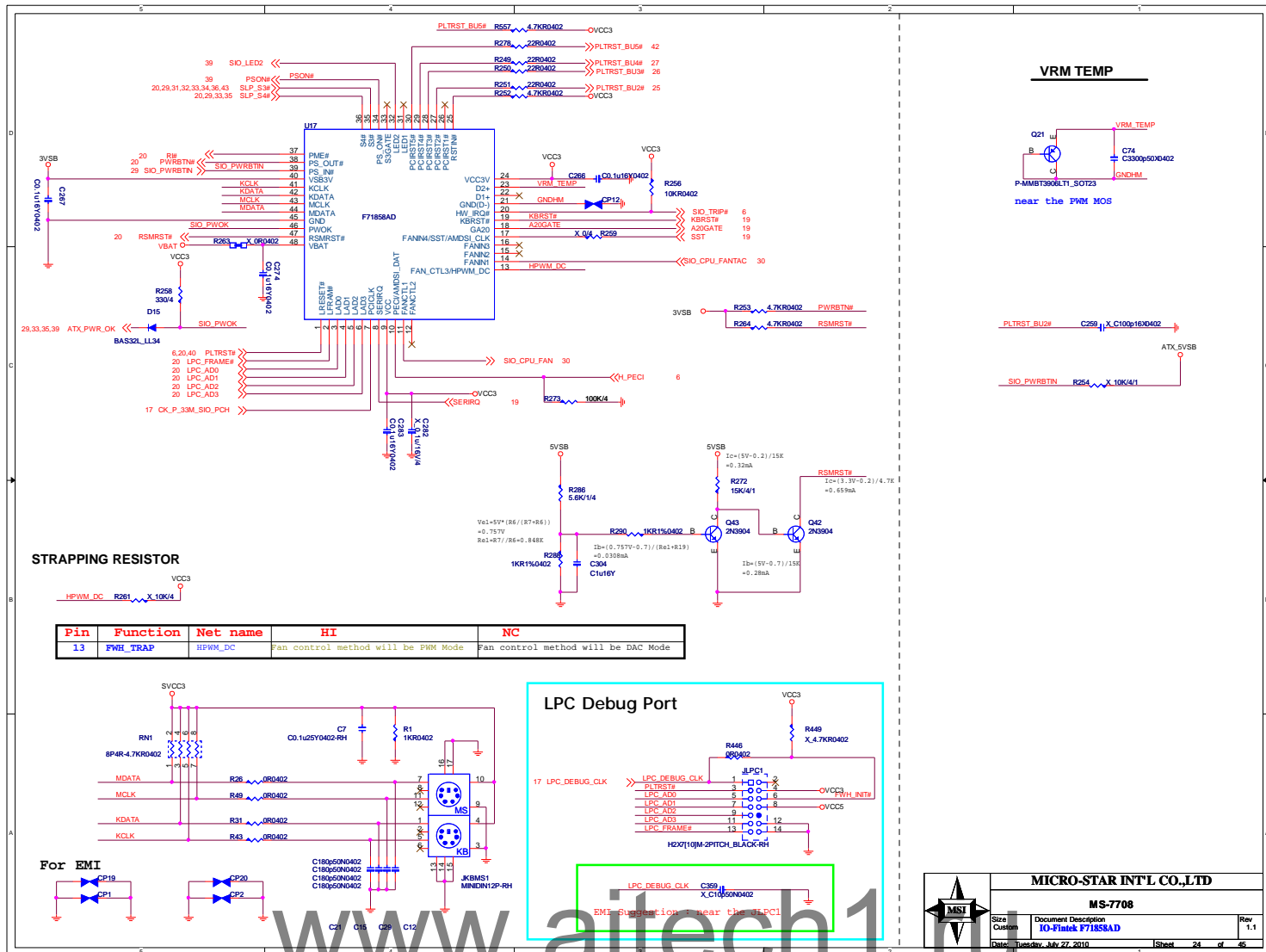




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Trace width > 200 mils

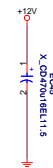
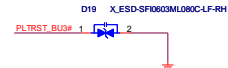
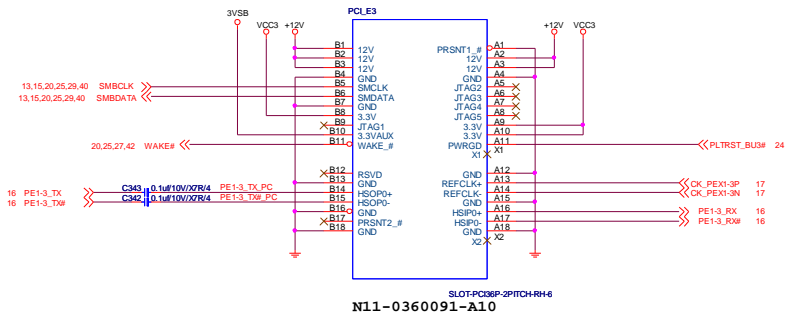
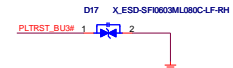
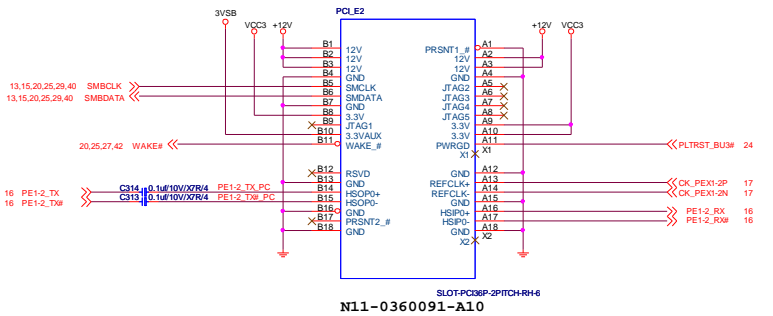


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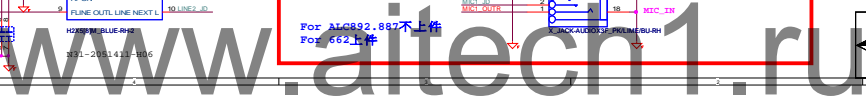
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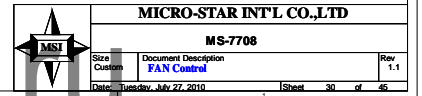
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For 892&887-VD
Fax 660-

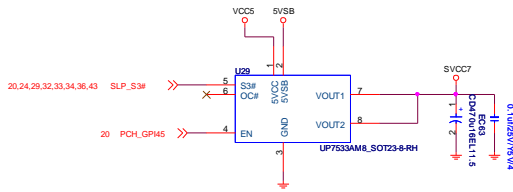


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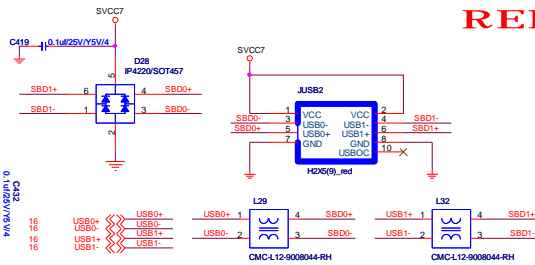
FRONT POWER CONTROL

POWER CIRCUIT FOR USB PORT 0, 1



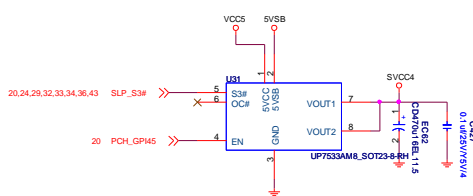
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

RED



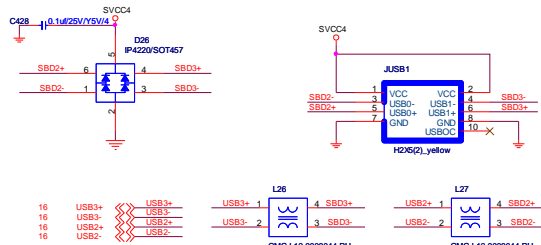
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 2, 3



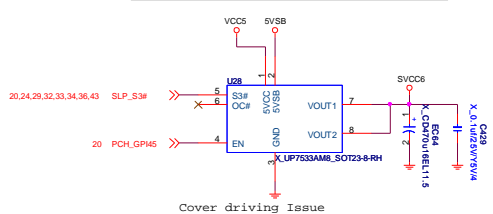
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

YELLOW



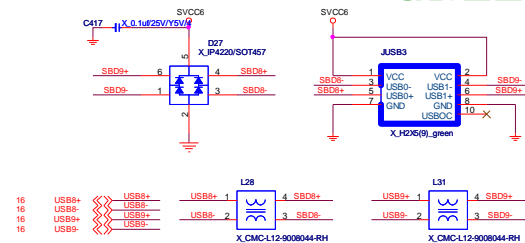
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 8, 9



FRONT PANEL USB CONNECTOR FOR USB PORT 8, 9

GREEN



NEAR USB CONNECTOR

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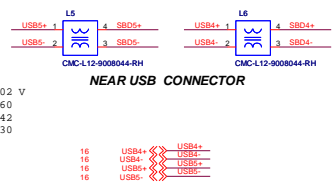
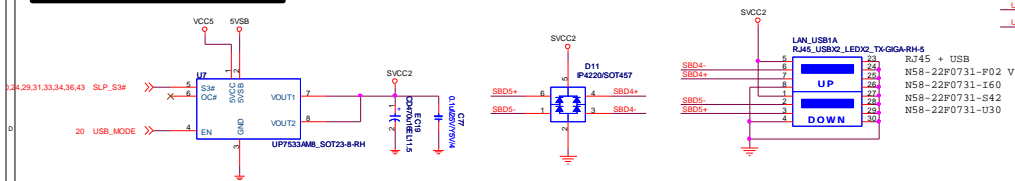
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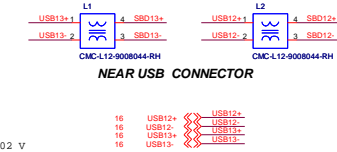
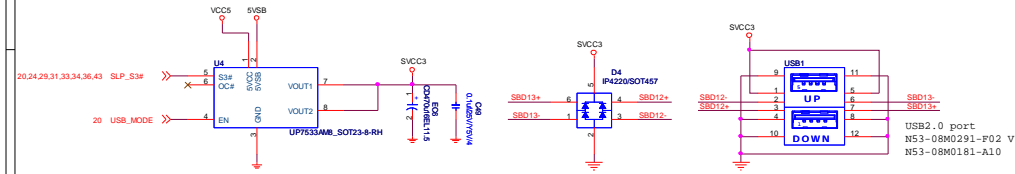
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REAR POWER CONTROL

REAR PANEL USB/LAN CONNECTOR FOR USB PORT 4,5

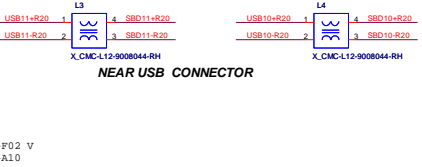
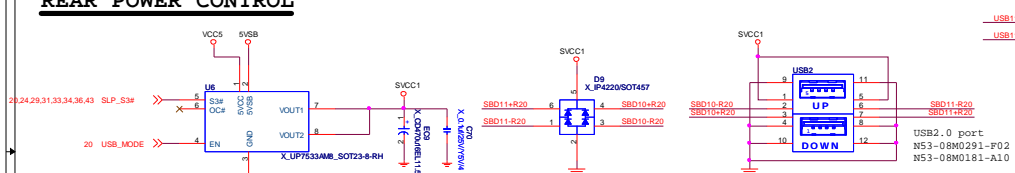


REAR PANEL USB/KB CONNECTOR FOR USB PORT 12,13



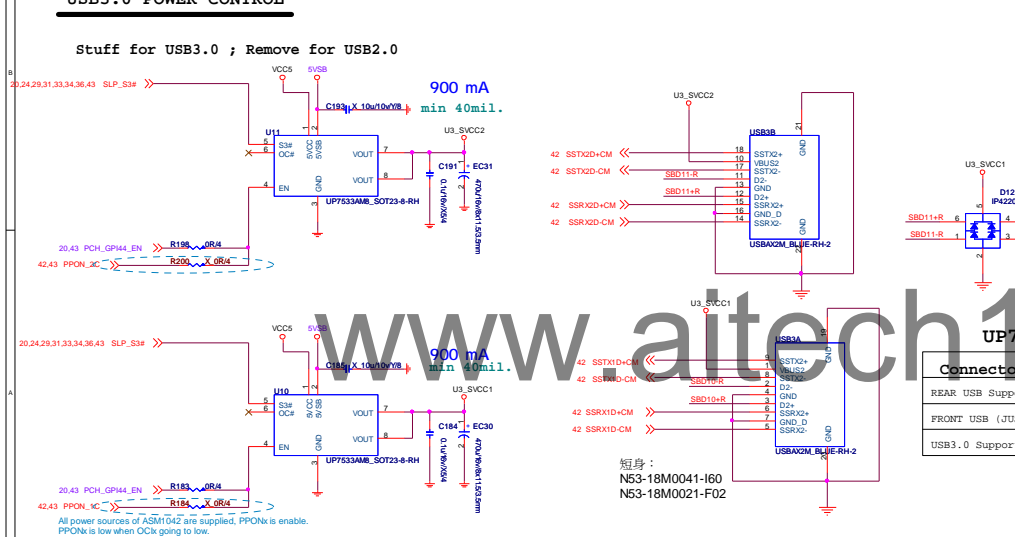
REAR POWER CONTROL

REAR PANEL USB/LAN CONNECTOR FOR USB PORT 10,11(Colay USB3.0) *option



USB3.0 POWER CONTROL

REAR PANEL USB CONNECTOR FOR USB PORT 10,11(Colay USB3.0)

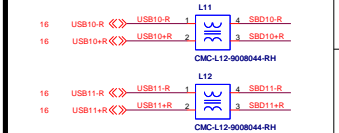


Stuff for USB2.0

USB11-R R212 X OR4 USB11-R20
USB11-R R211 X OR4 USB11-R20
USB10-R R210 X OR4 USB10-R20
USB10-R R205 X OR4 USB10-R20

NEAR REAR USB CONNECTOR

Stuff for USB3.0



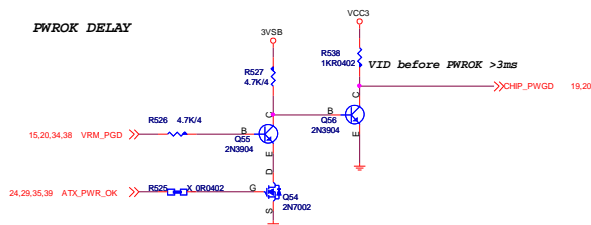
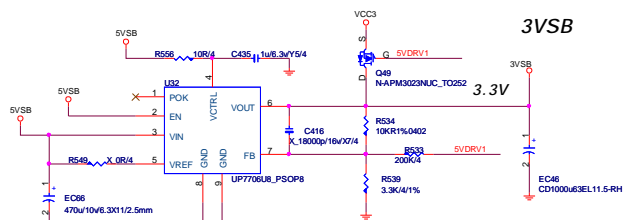
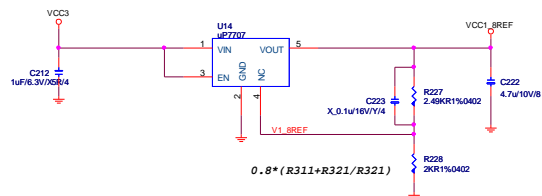
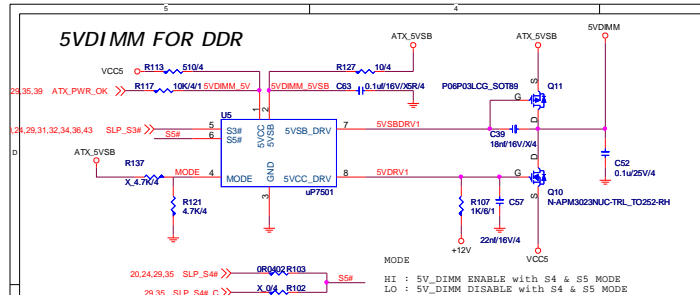
UP7533 ENABLE CONTROL

Connector	Power	GPIO Control
REAR USB Support S5 Power (KB/PS2/LAN)	SVCC1, SVCC2, SVCC3	USB_MODE
FRONT USB (JUSB1, JUSB2, JUSB3, JUSB4)	SVCC4, SVCC6, SVCC7	PCH_GPI45
USB3.0 Support S5 Power	U3_SVCC1, U3_SVCC2	PCH_GPI44

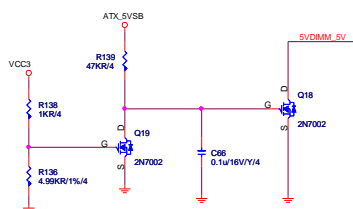


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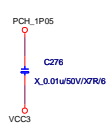
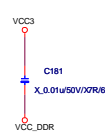
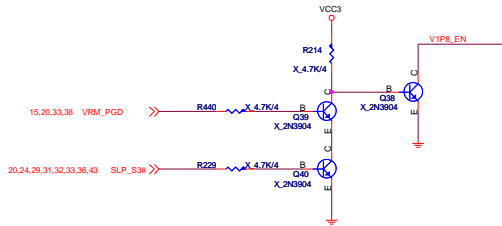
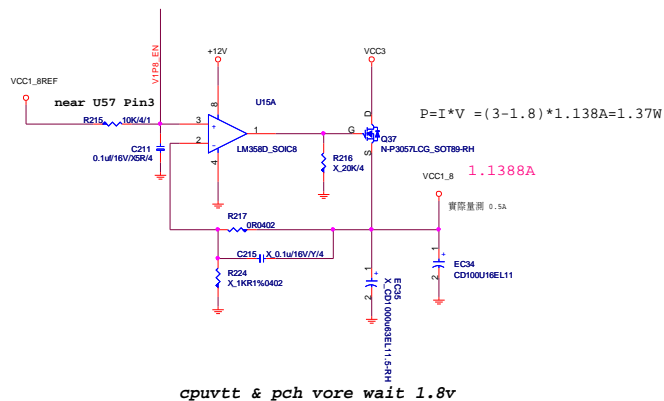


Update from SLP S3# to VRM PGD



For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.





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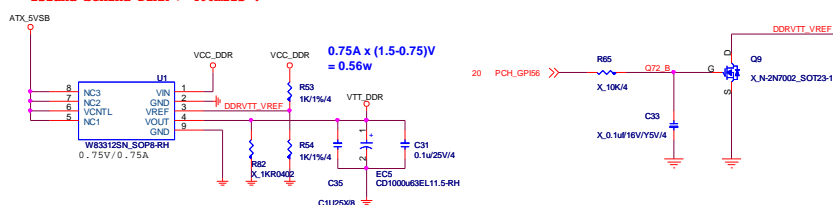
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DDR3_1.5V

8A

21.65A



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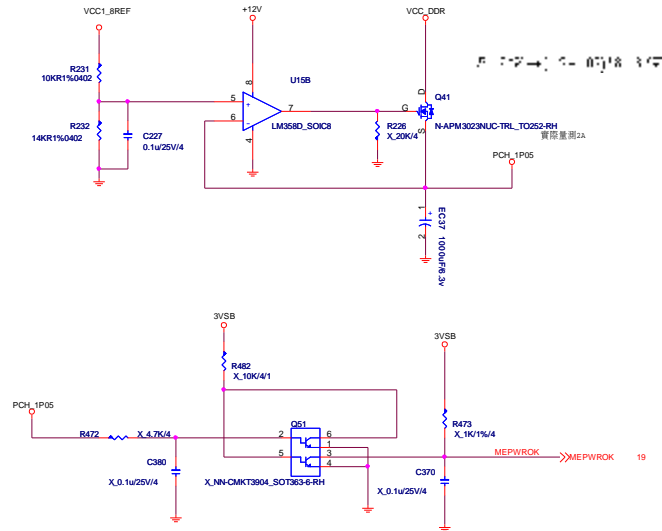
CPU_VTT

$$\begin{aligned} P &= I_{in} \cdot V_{in} = I_{out} \cdot V_{out} \\ 30 \cdot 1.2 &= I_{out} \cdot 12 \cdot 0.8 \\ I_{out} &= 3.75A = 150mil \quad (1A = 40mil) \end{aligned}$$


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	Size Custom	Document Description CPU_VTT - NCP1589A_1-Phase	Rev 1.1
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PCH Core

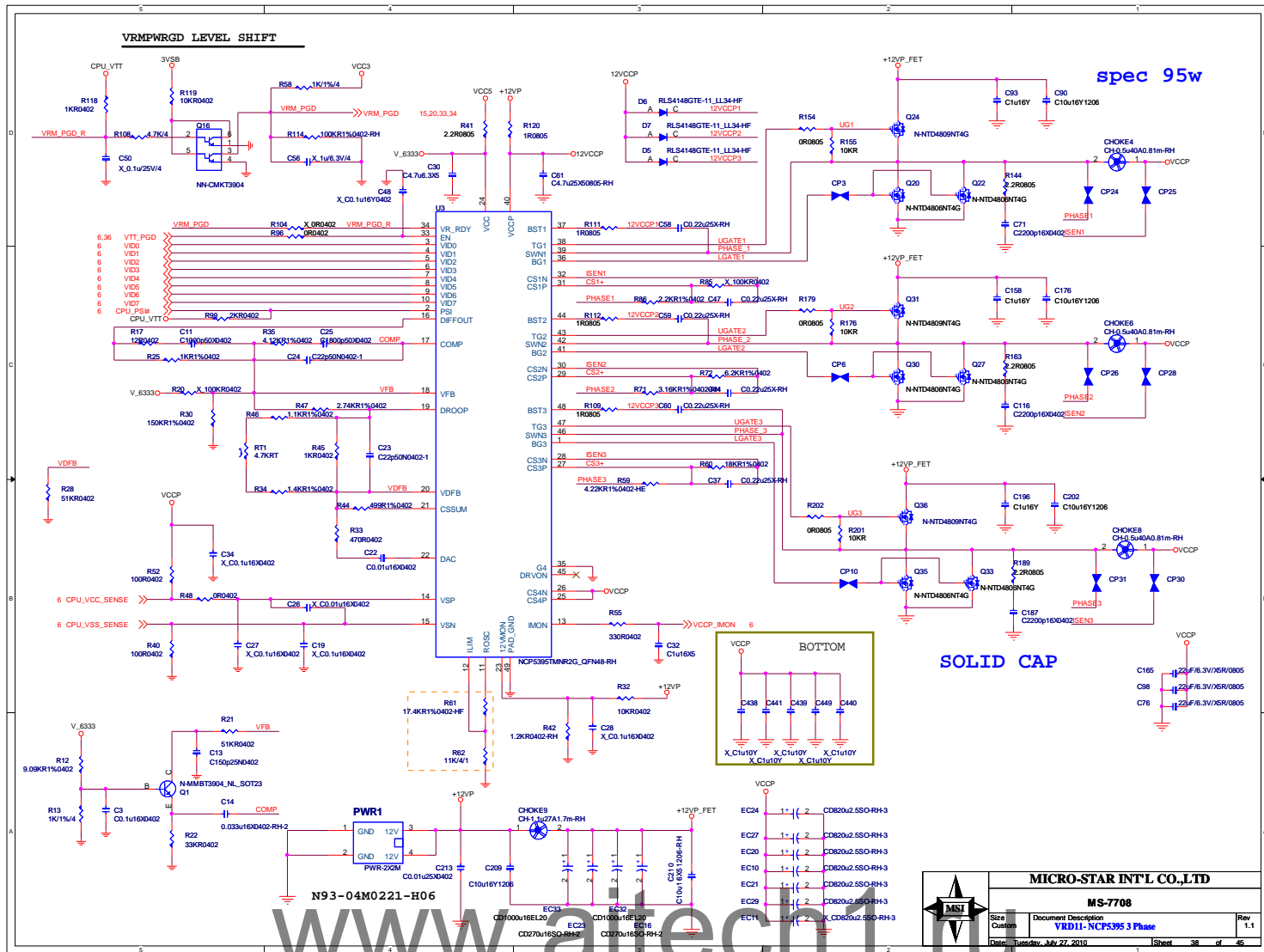
$$5.5A(PCH) + 2.5A(VCCME) = 8A$$

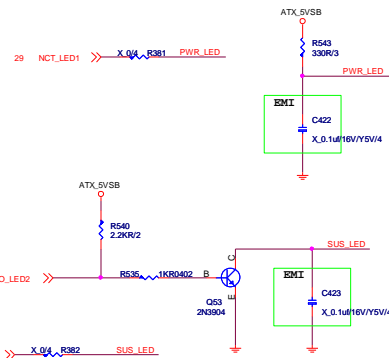
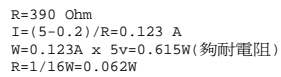
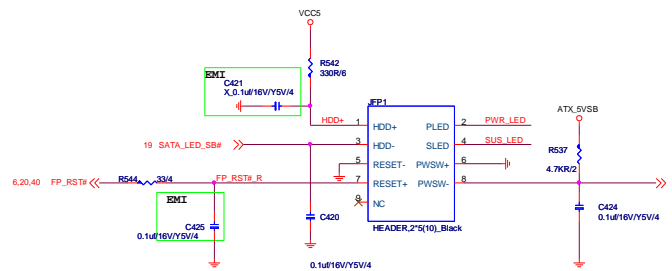
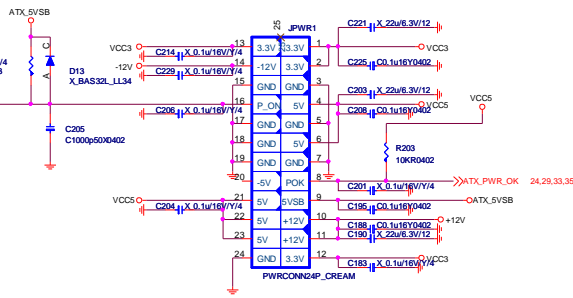


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Size Custom	Document Description PCH POWER - LM358	Rev 1.1
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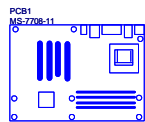


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PCB



P30-0770811-E55, 依頓 V
P30-0770811-G37, 精成

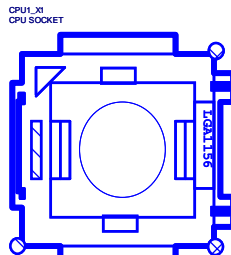


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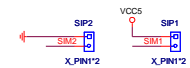
BAT-BCR2032P-RH

CPU SOCKET

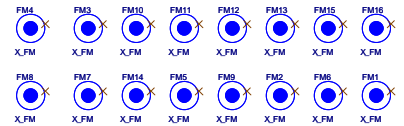


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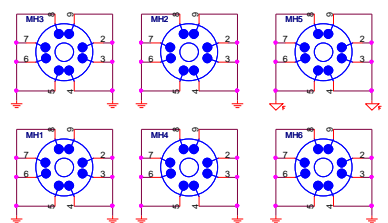
Simulation



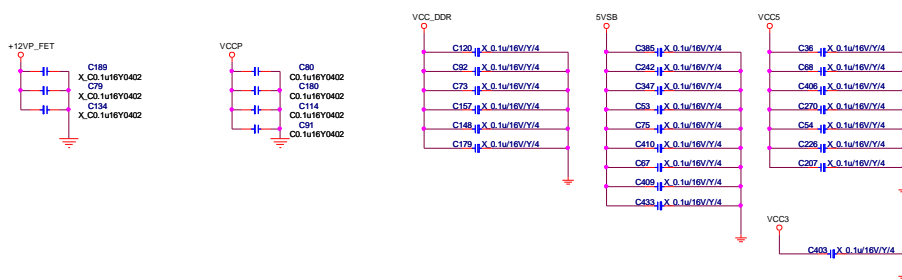
Optical Fiducial Marks-120



Mounting Holes



For EMI



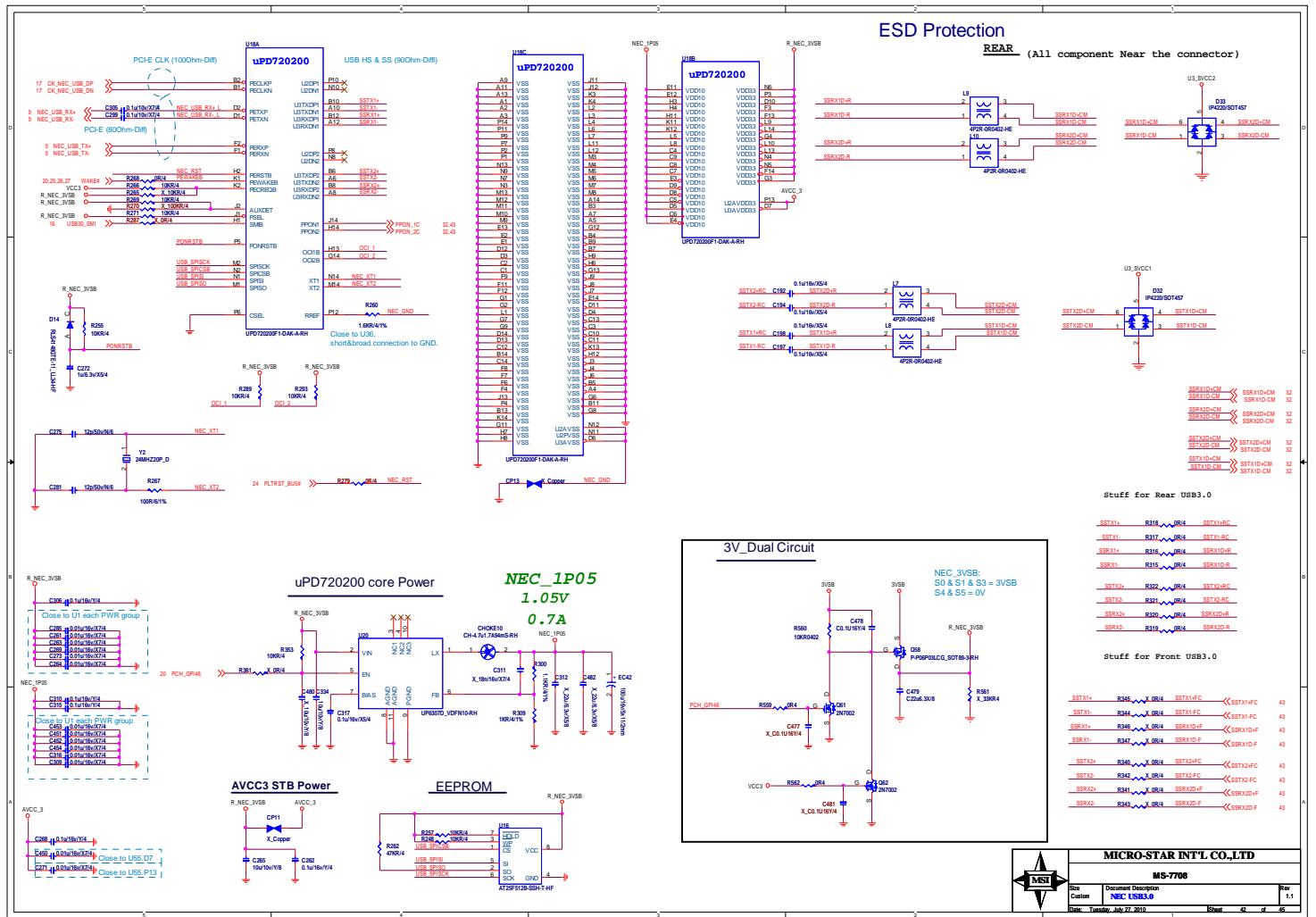
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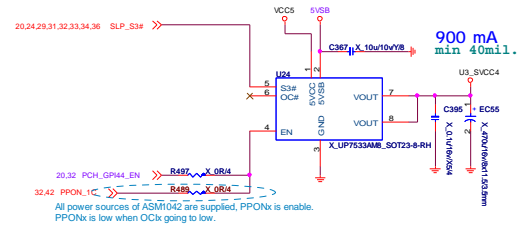
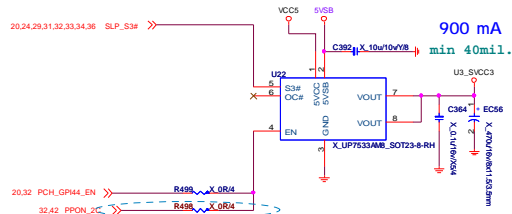
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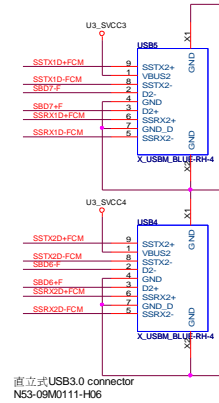
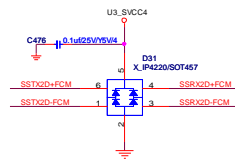
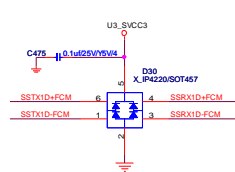
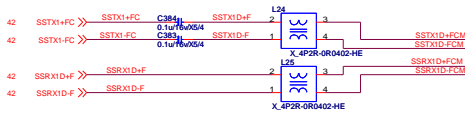
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Stuff for USB3.0 ; Remove for USB2.0

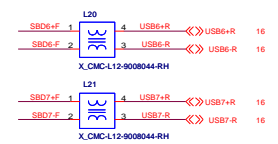
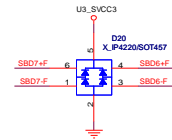


FRONT PANEL USB CONNECTOR
FOR USB PORT 12,13

FRONT (All component Near the connector)



NEAR FRONT USB CONNECTOR



直立式USB3.0 connector
N53-09M0111-H06

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